IN THE DRAWINGS:

The attached sheet of drawings is new Fig. 11.

Attachment: **New Figure**

REMARKS

This amendment is submitted in response to the Office Action dated March 15, 2007. Reconsideration and allowance of the claims are requested. In the Office Action, at paragraph 1, the Examiner requested that Figure 3 be designated as prior art. This rejection is respectfully traversed. The specification clearly states at page 7, that Figure 3 is a code tree in accordance with the embodiment of the present invention. Therefore, the undersigned cannot make the suggested amendment without expressly contradicting a statement in the application, as filed and approved by the inventor.

The drawings are objected to as failing to show the method of claims 11, 21 and 30. Therefore, a new Figure 11 is submitted herewith, and an appropriate amendment has been made to the specification. It is noted that there is no pending rejection for lack of support for the claims, and a review of the specification shows that the claimed subject matter is already clearly described to one of skill in the art. Therefore, entry of the Figures and the corresponding description is respectfully requested since no new matter is involved.

At pages 3 and 4 of the Office Action, the Examiner requested certain changes to the specification. These changes have been made, except for the change to paragraphs 16 and 34 and the second change to paragraph 58, where it is submitted the language is accurate as is. Also, the last paragraph of the Office Action at page 4 is not understood, so no action has been taken.

The Examiner objects to claims 1 and 21 as being informal and unclear. Therefore, these claims have been amended. The Examiner has objected to claims 18-20, 27-29 and 40-42. Therefore these claims have been withdrawn. The Examiner has objected to claims 2-5 and 11-42 as lacking clarity. These claims have been amended. The Examiner rejects claims 1, 5, 6, 21-23 and 27 under 35 USC §102(b) as anticipated by Dabiri (US 5,996,112). The Examiner also rejects 2-4, 9, 24-26, 28-35 and 40-42 under 35 USC 103(a) as obvious and unpatentable over Dabiri. These rejections are respectfully traversed. The Examiner also indicates that claims 7, 8, 10-20 and 36-39 would be allowable if rewritten to deal with the issues described above. This allowability is noted.

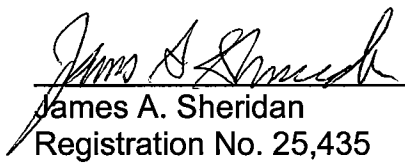
The Applicant respectfully submits that the claims, as now amended, clearly describe a system that is significantly different than the prior art. As now recited in all of the independent claims, the present invention provides a method and an apparatus for implementing a trace-back process in a Viterbi decoder for tracing back a most likely path through a code tree for decoding convolutional encoded data. As stated at paragraph [0049] of the present application, in the ideal decoder, of which Dabiri is an example, the survivor memory is sufficiently wide to provide for all possible sample states. The survivor bits help to trace back the states as the path is traversed and are called in succession from the memory. This is what is disclosed at Dabiri, relative to the buffer 226. In fact, buffer 226 is a single stage buffer, which means that all survivor bits are stored as a single word.

To the contrary, in the claimed invention, the survivor bits for all even states are stored at an even addressed word, and survivor bits for all odd states are stored in an odd addressed word Dabiri's buffer 226, as a single stage buffer, is clearly incapable of implementing this feature. Further, the present invention differs from Dabiri in several other ways that are recited in the claims. The claims recite a pipelined architecture to access the memory, in spite of the fact, as clearly spelled out at paragraphs [0054] and [0055] of the application, that due to timing constraints and available technology, it would normally be expected that there would be performance degradation associated with the trace-back phase. To account for this and to compensate for the delay which would otherwise be introduced by pipeline registers, the survivor bits are stored in multiple memory words. Further, each of the trace bits defined using the survivor word is used to address one of the multiple memory words and to control the access of the addressed memory word.

By using this unique approach, the read address may be delayed to equalize pipeline skew by partitioning the memory to maintain data integrity, while enhancing and optimizing the throughput wait.

In view of the fact that all features are now clearly spelled out in the claims as presented, reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,



James A. Sheridan
Registration No. 25,435
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)